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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,799	HENRY ET AL.	
	Examin r	Art Unit	
	Tonia L Meonske	2183	

-- Th MAILING DATE of this communication appears on th cov r sh t with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30, 34-39, and 45-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30, 34-39, and 45-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 15-30, 34-39, 45, 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al., US Patent 5,353,421 in view of Forster et al., US Patent 4,181,942.

3. Referring to claim 1, Emma et al. have taught a branch prediction apparatus in a processor including address selection logic for providing a fetch address to an instruction cache, the fetch address used to select lines of the instruction cache, the apparatus comprising:

a. first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic (abstract, Figure 10, elements 12 and 55, column 4, lines 1-44);

b. instruction decode logic, configured to receive and decode said branch instruction and to generate a type thereof (abstract, Figure 10, element 17); and

c. branch control logic, configured to control the address selection logic to select said first prediction as the fetch address, said first prediction selecting a first line of the instruction cache (Figure 10, abstract, column 4, lines 1-44, column 7, lines 3-12);

d. wherein said branch control logic is further configured to subsequently selectively control the address selection logic, based on said branch instruction type, to select said

second prediction as the fetch address, said second prediction selecting a second line of the instruction cache (Figure 10, abstract, column 4, lines 1-44, column 5, lines 35-68, column 17, lines 25-55).

4. Emma et al. have not taught providing two branch predictions for unconditional branch instructions. Specifically, the DHT of Emma et al., does not make predictions for unconditional branches. However, Emma et al. have taught substituting either of the branch predictors, including the DHT, with an op-code type branch predictor, such as that taught by Forster et al. in US Patent 4,181,942 (Emma et al., column 17, lines 25-36). Substituting the DHT of Emma et al. with the op-code type branch predictor of Forster et al. (Forster et al., Abstract, column 3, lines 28-56) results in two branch predictions for unconditional branch instructions. Having the DHT of Emma et al. instead be an op-code type branch predictor of Forster et al. would have been beneficial to control loops (Forster et al., Abstract, column 3, lines 28-56). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch predictor of Emma et al. (DHT), be replaced with the op-code type branch predictor of Forster et al. for the desirable purpose of controlling loops (Forster et al., Abstract, column 3, lines 28-56).

5. Referring to claim 2, Emma et al. have taught the apparatus of claim 1, as described above, and further comprising:

a. comparison logic, coupled to said first and second branch predictors, for comparing said first and second target address predictions (Figure 10, abstract, column 17, lines 39-45, column 9, lines 20-65).

6. Referring to claim 15, Emma et al. have taught the apparatus of claim 2, as described above, and wherein said first and second predictors are also configured to provide said first and second target address predictions of a conditional branch instruction to the address selection logic, wherein said type includes a specification of whether said branch instruction is a conditional type branch instruction (column 11, lines 18-58).

7. Referring to claim 16, Emma et al. have taught the apparatus of claim 15, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a conditional branch instruction and said first and second predictions miscompare (column 11, lines 18-58, column 13, line 65-column 14, line 14).

8. Referring to claim 17, Emma et al. have taught the apparatus of claim 15, as described above, and wherein said first and second predictors provide first and second direction predictions of said conditional branch instruction to said branch control logic for predicting whether said conditional branch instruction will be taken (column 11, line 66-column 12, line 30).

9. Referring to claim 18, Emma et al. have taught the apparatus of claim 17, as described above, and further comprising:

a. second comparison logic, coupled to said first and second branch predictors, for comparing said first and second direction predictions of said conditional branch instruction (Figure 10, abstract, column 17, lines 39-45, column 9, lines 20-65).

10. Referring to claim 19, Emma et al. have taught the apparatus of claim 18, wherein said branch control logic controls the address selection logic to select an instruction pointer of a next sequential instruction to said conditional branch instruction as the fetch address if said second

direction prediction predicts said conditional branch instruction will not be taken (column 12, lines 16-30).

11. Referring to claim 20, Emma et al. have taught the apparatus of claim 19, as described above, and wherein said branch control logic controls the address selection logic to select said next sequential instruction pointer if said second direction prediction predicts said conditional branch instruction will not be taken and said first and second direction predictions miscompare (column 12, lines 16-30).

12. Referring to claim 21, Emma et al. have taught the apparatus of claim 2, as described above, and wherein said branch control logic subsequently selectively controls the address selection logic based on said branch instruction type to select said second prediction as the fetch address if said first and second predictions do not match (Figure 10, abstract, column 4, lines 1-44, column 5, lines 35-68, column 17, lines 25-55).

13. Referring to claim 22, Emma et al. have taught the apparatus of claim 1, as described above. Emma et al. have not specifically taught wherein said branch instruction type comprises an Intel IA-32 instruction set branch instruction type. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch instructions of Emma et al. be implemented as any type of branch instruction, including and Intel IA-32 instruction set branch instruction, for the desirable purpose implementing and benefiting from this invention in a widely used instruction set.

14. Referring to claim 23, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor receives the instruction cache fetch address and

provides said first target address prediction in response to the fetch address (abstract, Figure 10, column 7, lines 3-32).

15. Referring to claim 24, Emma et al. have taught the apparatus of claim 23, as described above, and wherein said first branch predictor provides said first target address prediction in response to the fetch address whether or not an unconditional branch instruction is present in a third line of the instruction cache, said third instruction cache line selected subsequent to selection of said first instruction cache line (abstract, column 17, lines 39-55).

16. Referring to claim 25, Emma et al. have taught the apparatus of claim 23, as described above, and wherein said first branch predictor provides said first target address prediction prior to said instruction decode logic decoding said unconditional branch instruction (abstract, column 4, line 1-44).

17. Referring to claim 26, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor comprises a branch target address cache indexed by the instruction cache fetch address (column 7, line 54-column 8, line 22).

18. Referring to claim 27, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor comprises a speculative call/return stack (column 8, lines 23-55).

19. Claim 43 does not recite limitations above the claimed invention set forth in claim 15 and is therefore rejected for the same reasons set forth in the rejection of claim 15 above.

20. Claims 28, 29 30, 34, 35, 36, 39, and 45 do not recite limitations above the claimed invention set forth in claims 1 and 2 and are therefore rejected for the same reasons set forth in the rejection of claims 1 and 2 above.

21. Referring to claim 37, Emma et al. have taught the processor of claim 36, as described above, and further comprising:

a. an instruction cache, coupled to an address bus for receiving a fetch address, said fetch address selecting a line of instructions for provision to said instruction decode logic (Figure 10, elements 13, 11, 16, an 17).

22. Referring to claim 38, Emma et al. have taught the processor of claim 37, as described above, and wherein said speculative branch predictor makes said speculative prediction even though a possibility exists that no branch instruction is present in said line of instructions (column 7, line 53-2column 8, line 22, A prediction is always made for each instruction. A miss in the BHT predicts the next sequential instruction.).

23. Claim 48 does not recite limitations above the claimed invention set forth in claims 1, 2, 15, and 16 and is therefore rejected for the same reasons set forth in the rejection of claim 1, 2, and 15, and 16 above.

24. Claim 50 does not recite limitations above the claimed invention set forth in claims 1, 2, 15, 17, 18, and 19 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 15, 17, 18, and 19 above.

25. Claims 3-5 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al., US Patent 5,353,421, in view of Forster et al., US Patent 4,181,942, and Gochman et al, US Patent 5,964,868.

26. Referring to claim 3, Emma et al. have taught the apparatus of claim 2 as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said branch instruction is a return type branch instruction. However Gochman et al.

have taught wherein said type includes a specification of whether said branch instruction is a return type branch instruction (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28) for the desirable purpose of implementing the speculative return stack buffer so that instructions can continue to be fetched while a main memory access occurs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al., include a specification of whether said branch instruction is return type branch instruction, as taught by Gochman et al., for the desirable purpose of being able to implement the speculative return stack buffer so that instructions can continue to be fetched while a main memory access occurs (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28).

27. Referring to claim 4, Emma et al. in combination with Gochman et al. have taught the apparatus of claim 3, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a return instruction and said first and second predictions miscompare (Gochman et al., column 7, lines 1-37, Emma et al., column 17, lines 13-5).

28. Referring to claim 5, Emma et al. in view of Gochman et al. have taught the apparatus of claim 4, as described above, and wherein said second branch predictor comprises a call/return stack for providing said second target address prediction of said return instruction (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28).

29. Claim 47 does not recite limitations above the claimed invention set forth in claims 1-4 and is therefore rejected for the same reasons set forth in the rejection of claims 1-4 above.

30. Claims 6-14, 46, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al., US Patent 5,353,421, in view of Forster et al., US Patent 4,181,942, and Rappoport et al., US Patent 6,601,161.

31. Referring to claim 6, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said unconditional branch instruction is a program counter-relative type branch instruction. Rappoport et al. have taught said type includes a specification of whether said branch instruction is a program counter-relative type branch instruction (Rappoport et al., column 9, line 50-column 10, line 42, column 2, lines 1-12) so that the predictor that predicts indirect branches, or program counter-relative branches, most accurately is used. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al., include a specification if whether said unconditional branch instruction is an program counter-relative branch type instruction as taught by Rappoport et al. for the desirable purpose of using the predictor that most accurately predicts program counter-relative branches (Rappoport et al., column 9, line 50-column 10, line 42, column 2, lines 1-12).

32. Referring to claim 7, Emma et al. in combination with Rappoport et al. have taught the apparatus of claim 6, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a program counter-relative branch instruction and said first and second predictions miscompare (Rappoport et al., line 50-column 10, line 42).

33. Referring to claim 8, Emma et al. have taught the apparatus of claim 7, as described above, and wherein said second branch predictor comprises an arithmetic unit for calculating

said second target address prediction based on an instruction pointer of said unconditional branch instruction (column 11, lines 1-17).

34. Referring to claim 9, Emma et al. have taught the apparatus of claim 8, as described above, and wherein said arithmetic unit calculates said second target address prediction using said instruction pointer of said unconditional branch instruction (column 11, lines 1-17).

35. Referring to claim 10, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not taught wherein said type includes a specification of whether said unconditional branch instruction is a direct type branch instruction. However, Rappoport et al. have taught wherein said type includes a specification of whether said branch instruction is a direct type branch instruction (Rappoport et al., column 9, line 10-column 10, line 66) for the desirable purpose of using the predictor that will most likely predict the direct branch correctly. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al, includes a specification of whether said unconditional branch instruction is a direct type branch instruction, as taught by Rappoport et al. for the desirable purpose of using the predictor that will most likely predict the direct branch correctly.

36. Referring to claim 11, Emma et al. have taught the apparatus of claim 10, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a direct branch instruction and said first and second predictions miscompare (column 13, line 67-column 14, line 14).

37. Referring to claim 12, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said unconditional branch instruction is an indirect type branch instruction. However,

Rappoport et al. have taught wherein said type includes a specification of whether said branch instruction is an indirect type branch instruction (Rappoport et al., column 9, line 50-column 10, line 42) so that the predictor that predicts indirect branches most accurately is used. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al., include a specification if whether said unconditional branch instruction is an indirect branch type instruction as taught by Rappoport et al. for the desirable purpose of using the predictor that most accurately predicts indirect branches (Rappoport et al., column 9, line 50-column 10, line 42).

38. Referring to claim 13, Emma et al. in view of Rappoport et al. have taught the apparatus of claim 12, as described above, and wherein said branch control logic controls the address selection logic not to select said second target address prediction if said branch instruction type is an indirect branch instruction (Rappoport et al., line 50-column 10, line 42).

39. Referring to claim 14, Emma et al. have taught the apparatus of claim 13, as described above, and wherein said second branch predictor comprises a branch target buffer for caching branch target addresses of previously executed indirect branch instructions (Rappoport et al., line 50-column 10, line 42).

40. Claim 46 does not recite limitations above the claimed invention set forth in claims 1, 2, 6, and 7 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 6, and 7 above.

41. Claim 49 does not recite limitations above the claimed invention set forth in claims 1, 2, 12, 13, and 14 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 12, 13, and 14 above.

Response to Arguments

42. Applicant's arguments with respect to claims 1-50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

44. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

46. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER